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Conference
Proceeding

IEEE
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IEEE Standard

- ☐ 1. **A low overhead design for testability and test generation technique for core-based systems-on-a-chip**
Ghosh, I.; Jha, N.K.; Dey, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 18, Issue 11, Nov. 1999 Page(s):1661 - 1676
Digital Object Identifier 10.1109/43.806811
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(352 KB) IEEE JNL
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- ☐ 2. **Hierarchical test generation and design for testability method: ASPPs and ASIPs**
Ghosh, I.; Raghunathan, A.; Jha, N.K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 18, Issue 3, March 1999 Page(s):357 - 370
Digital Object Identifier 10.1109/43.748165
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(368 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. **TAO: regular expression-based register-transfer level testability analysis and optimization**
Ravi, S.; Lakshminarayana, G.; Jha, N.K.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 9, Issue 6, Dec. 2001 Page(s):824 - 832
Digital Object Identifier 10.1109/92.974896
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(229 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 4. **Software-based self-test methodology for crosstalk faults in processors**
Xiaoliang Bai; Li Chen; Dey, S.;
High-Level Design Validation and Test Workshop, 2003. Eighth IEI

International
2003 Page(s):11 - 16
Digital Object Identifier 10.1109/HLDVT.2003.1252468
[AbstractPlus](#) | [Full Text: PDF\(524 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ **5. A scalable software-based self-test methodology for programmable processors**
Li Chen; Ravi, S.; Raghunathan, A.; Dey, S.;
[Design Automation Conference, 2003. Proceedings](#)
2-6 June 2003 Page(s):548 - 553
[AbstractPlus](#) | [Full Text: PDF\(943 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **6. TAO: regular expression based high-level testability analysis : optimization**
Ravi, S.; Lakshminarayana, G.; Jha, N.K.;
[Test Conference, 1998. Proceedings. International](#)
18-23 Oct. 1998 Page(s):331 - 340
Digital Object Identifier 10.1109/TEST.1998.743171
[AbstractPlus](#) | [Full Text: PDF\(1052 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **7. TAO-BIST: A framework for testability analysis and optimization for built-in self-test of RTL circuits**
Ravi, S.; Lakshminarayana, G.; Jha, N.K.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
Volume 19, Issue 8, Aug. 2000 Page(s):894 - 906
Digital Object Identifier 10.1109/43.856976
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(280 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **8. TAO-BIST: a framework for testability analysis and optimization of RTL circuits for BIST**
Ravi, S.; Jha, N.K.; Lakshminarayana, G.;
[VLSI Test Symposium, 1999. Proceedings. 17th IEEE](#)
25-29 April 1999 Page(s):398 - 406
Digital Object Identifier 10.1109/VTEST.1999.766695
[AbstractPlus](#) | [Full Text: PDF\(208 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **9. Test-Volume Reduction in Systems-on-a-Chip Using Heterogeneous and Multilevel Compression Techniques**
Lingappan, L.; Ravi, S.; Raghunathan, A.; Jha, N.K.; Chakradhar, S.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
Volume 25, Issue 10, Oct. 2006 Page(s):2193 - 2206
Digital Object Identifier 10.1109/TCAD.2005.862735
[AbstractPlus](#) | [Full Text: PDF\(832 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **10. Techniques for formal verification of digital systems: a system approach**
Shojaei, H.; Ghayoumi, H.;
[Digital System Design, 2004. DSD 2004. Euromicro Symposium on](#)
31 Aug.-3 Sept. 2004 Page(s):444 - 449
Digital Object Identifier 10.1109/DSD.2004.1333309
[AbstractPlus](#) | [Full Text: PDF\(294 KB\)](#) IEEE CNF

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- ☐ **11. A distributed computer architecture for qualitative simulation based on a multi-DSP and FPGAs**
Platzner, M.; Rinner, B.; Weiss, R.;
Parallel and Distributed Processing, 1995. Proceedings. Euromicro Workshop on
25-27 Jan. 1995 Page(s):311 - 318
Digital Object Identifier 10.1109/EMPDP.1995.389193
[AbstractPlus](#) | [Full Text: PDF\(428 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)

- ☐ **12. Custom-instruction synthesis for extensible-processor platfo**
Fei Sun; Ravi, S.; Raghunathan, A.; Jha, N.K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 23, Issue 2, Feb. 2004 Page(s):216 - 228
Digital Object Identifier 10.1109/TCAD.2003.822133
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(448 KB\)](#) **IEEE JNL**
[Rights and Permissions](#)

- ☐ **13. Behavioral-level synthesis of heterogeneous BISR reconfigur ASIC's**
Guerra, L.M.; Potkonjak, M.; Rabaey, J.M.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions
Volume 6, Issue 1, March 1998 Page(s):158 - 167
Digital Object Identifier 10.1109/92.661258
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(180 KB\)](#) **IEEE JNL**
[Rights and Permissions](#)

- ☐ **14. High level software synthesis for signal processing systems**
Ritz, S.; Pankert, M.; Meyr, H.;
Application Specific Array Processors, 1992. Proceedings of the International Conference on
4-7 Aug. 1992 Page(s):679 - 693
Digital Object Identifier 10.1109/ASAP.1992.218536
[AbstractPlus](#) | [Full Text: PDF\(712 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)

- ☐ **15. A formal approach to MpSoC performance verification**
Richter, K.; Jersak, M.; Ernst, R.;
Computer
Volume 36, Issue 4, April 2003 Page(s):60 - 67
Digital Object Identifier 10.1109/MC.2003.1193230
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(365 KB\)](#) **IEEE JNL**
[Rights and Permissions](#)

- ☐ **16. The TACO protocol processor simulation environment**
Virtanen, S.; Lilius, J.;
Hardware/Software Codesign, 2001. CODES 2001. Proceedings of the Ninth International Symposium on
25-27 April 2001 Page(s):201 - 206
Digital Object Identifier 10.1109/HSC.2001.924676
[AbstractPlus](#) | [Full Text: PDF\(516 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)

- ☐ **17. Power efficient mediaprocessors: design space exploration**
Kin, J.; Chunho Lee; Mangione-Smith, W.H.; Potkonjak, M.;
Design Automation Conference, 1999. Proceedings. 36th

21-25 June 1999 Page(s):321 - 326
Digital Object Identifier 10.1109/DAC.1999.781334
[AbstractPlus](#) | [Full Text: PDF\(596 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ **18. Exploring the diversity of multimedia systems**
Johnson Kin; Chunho Lee; Mangione-Smith, W.H.; Potkonjak, M.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions
Volume 9, Issue 3, June 2001 Page(s):474 - 485
Digital Object Identifier 10.1109/92.929581
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(408 KB\)](#) IEEE JNL
[Rights and Permissions](#)

- ☐ **19. An energy-aware IP core design for the variable-length DCT/II targeting at MPEG4 shape-adaptive transforms**
Kuan-Hung Chen; Jiun-In Guo; Jinn-Shyan Wang; Ching-Wei Yeh
Jia-Wei Chen;
Circuits and Systems for Video Technology, IEEE Transactions on
Volume 15, Issue 5, May 2005 Page(s):704 - 715
Digital Object Identifier 10.1109/TCSVT.2005.846441
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1544 KB\)](#) IEEE JNL
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- ☐ **20. Micro-architecture generation and simulation from high-level synthesis environment**
Benmohammed, M.; Bourahla, M.; Merniz, S.;
Computer Systems and Applications, 2003. Book of Abstracts.
ACS/IEEE International Conference on
14-18 July 2003 Page(s):5
Digital Object Identifier 10.1109/AICCSA.2003.1227442
[AbstractPlus](#) | [Full Text: PDF\(153 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ **21. An evolution programming approach on multiple behaviors for the design of application specific programmable processors**
Wei Zhao; Papachristou, C.A.;
European Design and Test Conference, 1996. ED&TC 96.
Proceedings
11-14 March 1996 Page(s):144 - 150
Digital Object Identifier 10.1109/EDTC.1996.494140
[AbstractPlus](#) | [Full Text: PDF\(616 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ **22. A core generator for fully synthesizable and highly parameterizable RISC-cores for system-on-chip designs**
Berekovic, M.; Heistermann, D.; Pirsch, P.;
Signal Processing Systems, 1998. SIPS 98. 1998 IEEE Workshop
8-10 Oct. 1998 Page(s):561 - 568
Digital Object Identifier 10.1109/SIPS.1998.715818
[AbstractPlus](#) | [Full Text: PDF\(507 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ **23. High level synthesis for reconfigurable datapath structures**
Guerra, L.; Potkonjak, M.; Rabaey, J.;
Computer-Aided Design, 1993. ICCAD-93. Digest of Technical
Papers., 1993 IEEE/ACM International Conference on
7-11 Nov. 1993 Page(s):26 - 29
Digital Object Identifier 10.1109/ICCAD.1993.580026
[AbstractPlus](#) | [Full Text: PDF\(340 KB\)](#) IEEE CNF

Rights and Permissions

- ☐ **24. Hypermedia processors: design space exploration**
Kin, J.; Chunho Lee; Mangione-Smith, W.H.; Potkonjak, M.;
Multimedia Signal Processing, 1998 IEEE Second Workshop on
7-9 Dec. 1998 Page(s):323 - 328
Digital Object Identifier 10.1109/MMSP.1998.738954
AbstractPlus | Full Text: PDF(336 KB) IEEE CNF
Rights and Permissions
- ☐ **25. Power, performance and area exploration of block matching algorithms mapped on programmable processors**
Kroupis, N.; Dasigenis, M.; Argyriou, A.; Tatas, K.; Soudris, D.;
Thanailakis, A.; Zervas, N.; Goutis, C.E.;
Image Processing, 2001. Proceedings. 2001 International Conference on
Volume 3, 7-10 Oct. 2001 Page(s):728 - 731 vol.3
Digital Object Identifier 10.1109/ICIP.2001.958222
AbstractPlus | Full Text: PDF(376 KB) IEEE CNF
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